REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					

REV STATUS OF PAGES	**REV**																		
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 12-09-14	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, LINEAR, SINGLE SUPPLY, LOW POWER FET INPUT OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12636**
	REV	**PAGE** 1 **OF** 17

AMSC N/A

5962-V098-12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single supply, low power field effect transistor (FET) input operational microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12636	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD822	Single supply, low power FET input operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S)	±18 V
Input voltage (V_{IN})	$+V_S$ + 0.2 V to $-V_S$ – 20 V
Output short duration	Indefinite
Differential input voltage	±30 V
Internal power dissipation (P_D)	156.25 mW typical
Maximum junction temperature (TJ)	150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 60 seconds)	+260°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_S)	±15 V
Operating temperature range (T_A)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to case (θ_{JC})	43°C/W
Thermal resistance, junction to ambient (θ_{JA})	160°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_S = 0 V, 5 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance.							
Initial offset voltage	V_{IO}		+25°C	01		0.8	mV
			-55°C to +125°C			1.2	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	2 typical		µV/°C
Input bias current	I_{IB}	V_{CM} = 0 V to 4 V	+25°C	01		25	pA
			-55°C to +125°C			6	nA
Input offset current	I_{IO}		+25°C	01		20	pA
			-55°C to +125°C		0.5 typical		nA
Open loop gain	AO	V_{OUT} = 0.2 V to 4 V, R_L = 100 kΩ	+25°C	01	500		V/mV
			-55°C to +125°C		400		
		V_{OUT} = 0.2 V to 4 V, R_L = 10 kΩ	+25°C		80		
			-55°C to +125°C		80		
		V_{OUT} = 0.2 V to 4 V, R_L = 1 kΩ	+25°C		15		
			-55°C to +125°C		10		
Noise/harmonic performance.							
Input voltage noise	NV	f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		µVpp
		f = 10 Hz			25 typical		nV / $\sqrt{Hz}$
		f = 100 Hz			21 typical		
		f = 1 kHz			16 typical		
		f = 10 kHz			13 typical		
Input current noise	NI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		fApp
		f = 1 kHz			0.8 typical		fA / $\sqrt{Hz}$
Harmonic distortion		V_{OUT} = 0.25 V to 4.75 V, f = 10 kHz, R_L = 10 kΩ to 2.5 V	+25°C	01	-93 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 0 V, 5 V, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Unity gain frequency			+25°C	01	1.8 typical		MHz
Full power response		V_{OUT}pp = 4.5 V	+25°C	01	210 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/μs
Settling time	t_S	To 0.1%, V_{OUT} = 0.2 V to 4.5 V	+25°C	01	1.4 typical		μs
		To 0.01%, V_{OUT} = 0.2 V to 4.5 V			1.8 typical		
Matching characteristics.							
Initial offset voltage	V_{IO}		+25°C	01		1.0	mV
			-55°C to +125°C			1.6	
Initial offset voltage drift	ΔV_{IO}		+25°C	01	3 typical		μV/°C
Input bias current	I_{IB}		+25°C	01		20	pA
Crosstalk	CT	At f = 1 kHz, R_L = 5 kΩ	+25°C	01	-130 typical		dB
		At f = 100 kHz, R_L = 5 kΩ			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-0.2	+4	V
Common mode rejection ratio	CMRR	V_{CM} = 0 V to 2 V	+25°C	01	66		dB
			-55°C to +125°C		66		
Differential input impedance	Z		+25°C	01	10^{13}||0.5 typical		Ω||pF
Common mode input impedance	Z		+25°C	01	10^{13}||2.8 typical		Ω||pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = 0 V, 5 V, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics.							
Output saturation 3/ voltage		$V_{OL} – V_{EE}$, I_{SINK} = 20 μA	+25°C	01		7	mV
			-55°C to +125°C			10	
		$V_{CC} – V_{OH}$, I_{SOURCE} = 20 μA	+25°C			14	
			-55°C to +125°C			20	
		$V_{OL} – V_{EE}$, I_{SINK} = 2 mA	+25°C			55	
			-55°C to +125°C			80	
		$V_{CC} – V_{OH}$, I_{SOURCE} = 2 mA	+25°C			110	
			-55°C to +125°C			160	
		$V_{OL} – V_{EE}$, I_{SINK} = 15 mA	+25°C			500	
			-55°C to +125°C			1000	
		$V_{CC} – V_{OH}$, I_{SOURCE} = 15 mA	+25°C			1500	
			-55°C to +125°C			1900	
Operating output current	I_{OUT}		+25°C	01	15		mA
			-55°C to +125°C		12		
Capacitive load drive	C_L		+25°C	01	350 typical		pF
Power supply.							
Quiescent current			-55°C to +125°C	01		1.6	mA
Power supply rejection ratio	PSRR	$+V_S$ = 5 V to 15 V	+25°C	01	66		dB
			-55°C to +125°C		66		

See footnotes at end of table.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_S = ±5 V, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance.							
Initial offset voltage	V_{IO}		+25°C	01		0.8	mV
			-55°C to +125°C			1.5	
Initial offset voltage drift	ΔV_{IO}		+25°C	01	2 typical		µV/°C
Input bias current	I_{IB}	V_{CM} = -5 V to 4 V	+25°C	01		25	pA
			-55°C to +125°C			6	nA
Input offset current	I_{IO}		+25°C	01		20	pA
			-55°C to +125°C		0.5 typical		nA
Open loop gain	AO	V_{OUT} = -4 V to 4 V, R_L = 100 kΩ	+25°C	01	400		V/mV
			-55°C to +125°C		400		
		V_{OUT} = -4 V to 4 V, R_L = 10 kΩ	+25°C		80		
			-55°C to +125°C		80		
		V_{OUT} = -4 V to 4 V, R_L = 1 kΩ	+25°C		20		
			-55°C to +125°C		10		
Noise/harmonic performance.							
Input voltage noise	NV	f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		µVpp
		f = 10 Hz			25 typical		nV / $\sqrt{Hz}$
		f = 100 Hz			21 typical		
		f = 1 kHz			16 typical		
		f = 10 kHz			13 typical		
Input current noise	NI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		fApp
		f = 1 kHz			0.8 typical		fA / $\sqrt{Hz}$
Harmonic distortion		V_{OUT} = ±4.5 V, f = 10 kHz, R_L = 10 kΩ	+25°C	01	-93 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 5$ V, $V_{CM} = 0$ V, $V_{OUT} = 0$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Unity gain frequency			+25°C	01	1.9 typical		MHz
Full power response		V_{OUT}pp = 9 V	+25°C	01	105 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/μs
Settling time	t_S	To 0.1%, $V_{OUT} = 0$ V to ±4.5 V	+25°C	01	1.4 typical		μs
		To 0.01%, $V_{OUT} = 0$ V to ±4.5 V			1.8 typical		
Matching characteristics.							
Initial offset voltage	V_{IO}		+25°C	01		1.0	mV
			-55°C to +125°C			3	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	3 typical		μV/°C
Input bias current	I_{IB}		+25°C	01		25	pA
Crosstalk	CT	At f = 1 kHz, $R_L = 5$ kΩ	+25°C	01	-130 typical		dB
		At f = 100 kHz, $R_L = 5$ kΩ			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-5.2	+4	V
Common mode rejection ratio	CMRR	V_{CM} = -5 V to 2 V	+25°C	01	66		dB
			-55°C to +125°C		66		
Differential input impedance	Z		+25°C	01	10^{13}||0.5 typical		Ω||pF
Common mode input impedance	Z		+25°C	01	10^{13}||2.8 typical		Ω||pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 5$ V, $V_{CM} = 0$ V, $V_{OUT} = 0$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics.							
Output saturation 3/ voltage		$V_{OL} - V_{EE}$, $I_{SINK} = 20$ μA	+25°C	01		7	mV
			-55°C to +125°C			10	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 20$ μA	+25°C			14	
			-55°C to +125°C			20	
		$V_{OL} - V_{EE}$, $I_{SINK} = 2$ mA	+25°C			55	
			-55°C to +125°C			80	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 2$ mA	+25°C			110	
			-55°C to +125°C			160	
		$V_{OL} - V_{EE}$, $I_{SINK} = 15$ mA	+25°C			500	
			-55°C to +125°C			1000	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 15$ mA	+25°C			1500	
			-55°C to +125°C			1900	
Operating output current	I_{OUT}		+25°C	01	15		mA
			-55°C to +125°C		12		
Capacitive load drive	C_L		+25°C	01	350 typical		pF
Power supply.							
Quiescent current			-55°C to +125°C	01		1.6	mA
Power supply rejection ratio	PSRR	$V_S = \pm 5$ V to ± 15 V	+25°C	01	66		dB
			-55°C to +125°C		66		

See footnotes at end of table.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_S = \pm 15$ V, $V_{CM} = 0$ V, $V_{OUT} = 0$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance.							
Initial offset voltage	V_{IO}		+25°C	01		2	mV
			-55°C to +125°C			3	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	2 typical		µV/°C
Input bias current	I_{IB}	$V_{CM} = 0$ V	+25°C	01		25	pA
		$V_{CM} = -10$ V			40 typical		
		$V_{CM} = 0$ V	-55°C to +125°C			6	nA
Input offset current	I_{IO}		+25°C	01		20	pA
			-55°C to +125°C		0.5 typical		nA
Open loop gain	AO	$V_{OUT} = -10$ V to 10 V, $R_L = 100$ kΩ	+25°C	01	500		V/mV
			-55°C to +125°C		500		
		$V_{OUT} = -10$ V to 10 V, $R_L = 10$ kΩ	+25°C		100		
			-55°C to +125°C		100		
		$V_{OUT} = -10$ V to 10 V, $R_L = 1$ kΩ	+25°C		30		
			-55°C to +125°C		20		
Noise/harmonic performance.							
Input voltage noise	NV	f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		µVpp
		f = 10 Hz			25 typical		nV / $\sqrt{Hz}$
		f = 100 Hz			21 typical		
		f = 1 kHz			16 typical		
		f = 10 kHz			13 typical		
Input current noise	NI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		fApp
		f = 1 kHz			0.8 typical		fA / $\sqrt{Hz}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15$ V, $V_{CM} = 0$ V, $V_{OUT} = 0$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise/harmonic performance - continued.							
Harmonic distortion		$V_{OUT} = \pm 10$ V, f = 10 kHz, $R_L = 10$ kΩ	+25°C	01	-85 typical		dB
Dynamic performance.							
Unity gain frequency			+25°C	01	1.9 typical		MHz
Full power response		$V_{OUT}pp = 20$ V	+25°C	01	45 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/μs
Settling time	t_S	To 0.1%, $V_{OUT} = 0$ V to ±10 V	+25°C	01	4.1 typical		μs
		To 0.01%, $V_{OUT} = 0$ V to ±10 V			4.5 typical		
Matching characteristics.							
Initial offset voltage	V_{IO}		+25°C	01		3	mV
			-55°C to +125°C			4	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	3		μV/°C
Input bias current	I_{IB}		+25°C	01		25	pA
Crosstalk	CT	At f = 1 kHz, $R_L = 5$ kΩ	+25°C	01	-130 typical		dB
		At f = 100 kHz, $R_L = 5$ kΩ			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-15.2	+14	V
Common mode rejection ratio	CMRR	$V_{CM} = -15$ V to +12 V	+25°C	01	70		dB
			-55°C to +125°C		70		
Differential input impedance	Z		+25°C	01	10^{13}||0.5 typical		Ω||pF
Common mode input impedance	Z		+25°C	01	10^{13}||2.8 typical		Ω||pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15$ V, $V_{CM} = 0$ V, $V_{OUT} = 0$ V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics.							
Output saturation 3/ voltage		$V_{OL} - V_{EE}$, $I_{SINK} = 20$ μA	+25°C	01		7	mV
			-55°C to +125°C			10	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 20$ μA	+25°C			14	
			-55°C to +125°C			20	
		$V_{OL} - V_{EE}$, $I_{SINK} = 2$ mA	+25°C			55	
			-55°C to +125°C			80	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 2$ mA	+25°C			110	
			-55°C to +125°C			160	
		$V_{OL} - V_{EE}$, $I_{SINK} = 15$ mA	+25°C			500	
			-55°C to +125°C			1000	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 15$ mA	+25°C			1500	
			-55°C to +125°C			1900	
Operating output current	I_{OUT}		+25°C	01	20		mA
			-55°C to +125°C		15		
Capacitive load drive	C_L		+25°C	01	350 typical		pF
Power supply.							
Quiescent current			-55°C to +125°C	01		1.8	mA
Power supply rejection ratio	PSRR	$V_S = \pm 5$ V to ± 15 V	+25°C	01	70		dB
			-55°C to +125°C		70		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This is a functional specification. Amplifier bandwidth decreases when the input common mode voltage is driven in the range ($+V_S - 1$ V) to $+V_S$. Common mode error voltage is typically less than 5 mV with the common mode voltage set at 1 V below the positive supply.

3/ $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

Case X

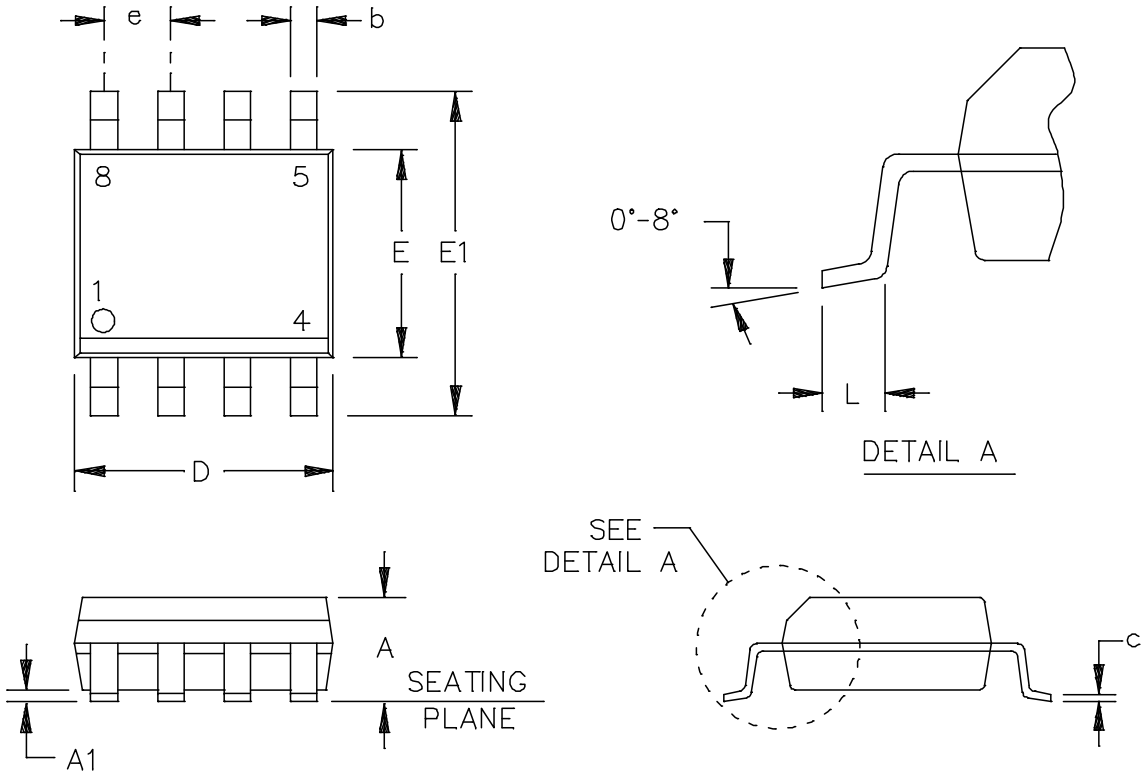

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12636
		REV	PAGE 14

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.053	.068	1.35	1.75
A1	.003	.009	0.10	0.25
b	.012	.020	0.31	0.51
c	.006	.009	0.17	0.25
D	.188	.196	4.80	5.00
E	.149	.157	3.80	4.00
E1	.228	.244	5.80	6.20
e	.049 BSC		1.27 BSC	
L	.015	.049	0.40	1.27

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUTPUT 1
2	-INPUT 1
3	+INPUT 1
4	$-V_S$
5	+INPUT 2
6	-INPUT 2
7	OUTPUT 2
8	$+V_S$

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12636-01XE	24355	AD822TRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland